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Defect-Limited Yield Difference Model

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Abstract This paper propose a novel yield difference model according to layout modification. The difference of average number of faults by layout modification to increase or decrease spaces between geometries is formulated for short faults and open faults. Complex modification including wire bending with jogs is also modeled by dividing patterns into segments and redefining spaces and widths. This model can help to monitor the yield change and to generate a cost function of defect-limited yield quickly.

요 약 본 논문은 레이아웃 수정에 따른 수율차 계산을 위한 새로운 모델을 제안한다. 패턴 사이의 빈 공간의 크기를 늘리거나 줄이는 레이아웃 변경으로 인한 결함 평균치의 차를 구하기 위한 식이 단락 결함과 개방 결함에 대해 제시 되었다. 미세 패턴인 조그를 포함한 구부러진 연결선등을 가지는 복잡한 레이아웃 변경은 패턴을 작은 조각으로 쪼개고 패턴 사이의 공간과 패턴의 폭을 재정의 함으로써 새롭게 모델링 하였다. 이 모델은 레이아웃 변경에 의한 수율 변화와 결함 제한적 수율에 대한 비용함수 모니터링을 쉽게 할 수 있다는 장점을 갖는다.

Key Words : defect-limited yield, layout modification

1. INTRODUCTION

The critical area of a VLSI design reflects the sensitivity of the layout to defect occurring and it has been used to predict the yield of a VLSI circuit. The critical area is defined as the region of the circuit layout in which the center of a circular defect has to fall in order to generate a circuit fault[1]. Defects are caused by particles such as dust and other contaminants in material and equipment. There are two types of defects: "extra material" defects causing short between two separate electrical nodes and "missing material" defects causing open circuit.[2] The extraction of critical area for both extra material defects and missing material defects cause the main computational bottleneck in yield prediction methodology.

The extraction mechanism originally proposed to determine missing critical area involved the extraction of the area of self intersection of a polygon shrunk by an amount equal to the defect radius. However, a simple polygon shrink will underestimate this area, since it not only shrinks across the width of the conduct as required, but also along its length as well. The critical area associated with the contacts should be combined with the region generated from the conductor itself to give the total critical area.

In this study, we propose a simple yield calculation method according to layout modification.

2. YIELD DIFFERENCE MODEL

There are a number of yield models reported in the literature relate fault probability to chip yield. A Poisson model which is often used with excellent results, since many fabrication processes have many layers and faults

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associated with each layer are largely independent.[3] The total defect-limited yield is defined as

$$Y_{Tot} = Y_0 \prod_{j=1}^{k} e^{-ANF(j)} \quad (1)$$

where Y_0 is factor which acts as an adjustment to take into account any non-random defects and ANF(j) is the average number of faults of type j. For single layer breaks and short[4], the expected value of ANF is defined as

$$ANF(j) = \int_{min(r)}^{max(r)} A(r)D(r)dr \quad (2)$$

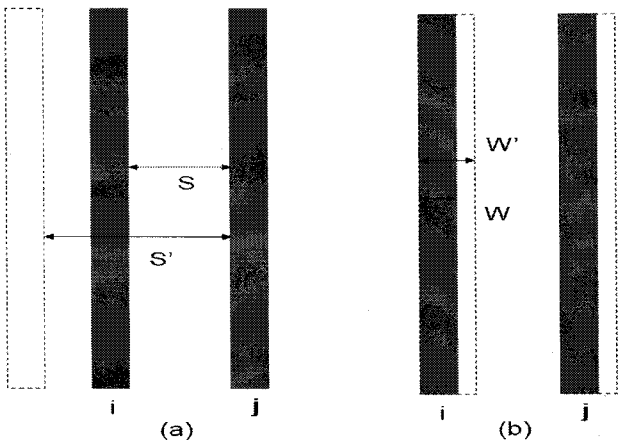
where A(r) denotes the area in which a defect of radius r causes circuit failure, and min(r) and max(r) represent smallest defect size and largest defect size of defect type j, respectively[5-8]. D(r) is the defect density function of the defect size which is also defined as $1/r^P$. P is a fall power (usually of the order 2-3). In this section, we propose the yield difference model with layout modification. We have studied two kinds of layout modifications such as simple modification and complex modification. For simple modification, layout geometries move to increase(or decrease) spaces between geometries for short fault. Layout geometries also expand itself to increase width of geometry for open fault. Complex layout modification includes bending of geometries as well as changes of space and width of simple modification.

2.1 Simple Layout Modification

In simple layout modification, we suppose that the layout geometries simply move horizontal or vertical direction without bending of geometry. Given a layout L, let S and W be spacing and width. After modification of the layout, S' and W' are new spacing and width as shown in Figure 1. Let $A(r)$ and $A'(r)$ be critical areas of layout L and L', respectively. Since the critical area should be larger than zero, A and A' of layouts L and L' is as follows.

$$A(r) = \begin{cases} \max\{(2r-S)l, 0\} & \text{for short fault,} \\ \max\{(2r-W)l, 0\} & \text{for open fault.} \end{cases} \quad (3)$$

$$A' = \begin{cases} \max\{(2r-S')l, 0\} & \text{for short fault,} \\ \max\{(2r-W')l, 0\} & \text{for open fault.} \end{cases} \quad (4)$$



[Figure 1] An example of simple layout modification: solid and dotted lines are a original layout and modified layout, respectively.

Since the defect-limited yield depends on the area causing average number of fault, the difference of yields directly associates the difference of *ANF = L'-L (DANF)* between two layouts geometries. The difference of ANF with respect to the short fault is generated by equation (3) and (4).

$$DANF(short) = \begin{cases} \int_{min(r)}^{S/2} 0D(r)dr & S \geq 2r \text{ and } S' \geq 2r, \\ \int_{S/2}^{S'/2} (S-2r)lD(r)dr & S < 2r \text{ and } S' \geq 2r, \\ \int_{S'/2}^{S/2} (2r-S')lD(r)dr & S \geq 2r \text{ and } S' < 2r, \\ \int_{S'/2}^{max(r)} (S-S')lD(r)dr & S < 2r \text{ and } S' < 2r. \end{cases} \quad (5)$$

However, due to limited area for layout modification, we expand the above formula to a new layout modification with bending wire and jogs. In addition, note that 2nd and 4th equations have negative value. Similarly, The difference of ANF with respect to the short fault is formulated as follows.

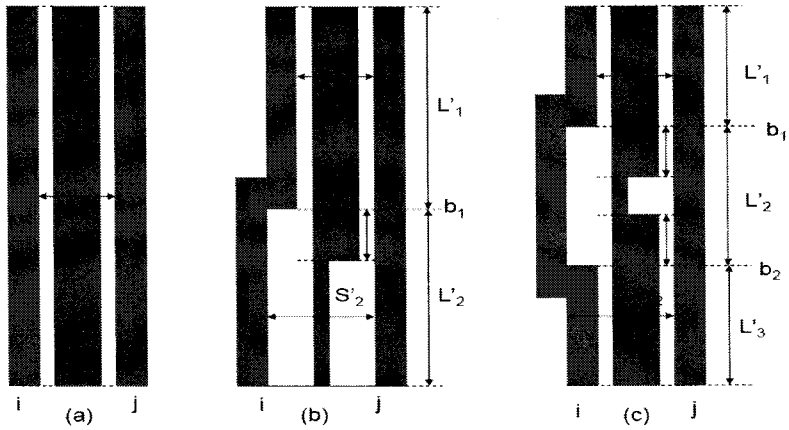
$$DANF(open) = \begin{cases} \int_{min(r)}^{W/2} 0D(r)dr & W \geq 2r \text{ and } W' \geq 2r, \\ \int_{W/2}^{W'/2} (W-2r)lD(r)dr & W < 2r \text{ and } W' \geq 2r, \\ \int_{W'/2}^{W/2} (2r-W')lD(r)dr & W \geq 2r \text{ and } W' < 2r, \\ \int_{W'/2}^{max(r)} (W-W')lD(r)dr & W < 2r \text{ and } W' < 2r. \end{cases} \quad (6)$$

2.2 Complex Layout Modification

Complex layout modification generates optimum layouts geometries for given a limited area of layout and thus uses wire bending technique. Geometries may have jogs after modification. For formulation of complex layout modification, we divide a pattern into segments and then define spaces and widths according to the segment. Given a layout L, let S and W be sets of spacings between segments and widths of segments, respectively. After modifying the layout, S' and W' are also defined as sets with modified spacings and widths of the new layout L'. n denotes the number of segments of a given layout.

Shape of critical area in complex modification is changed at bending point of wire, as shown in Figure 2. Thus, the formulations for difference of *ANF* are divided in terms of the bending point. L_1 in Figure 2(b) and L_1 and L_3 in Figure 2(c) follows the same formulation as the simple layout modification since the shape of critical area is not a polygon but a rectangular, i.e. no bending point in shape of critical area. The critical area had complex shapes as $S'_i < S'_{i+1}$. For example, critical area

in L_{i+1} of Figure 2(b) is divided by two intervals such as $[b_1, r]$ and $[r, L_{i+1}]$. The critical area in b_1 to r *of* L_{i+1} is the same as the result in L_i. The critical area in $[r,L_{i+1}]$ can be newly generated depending on S_{i+1} and S'_{i+1}. We show an example in conditions of $\{S_i,S_{i+1}\} < 2r$ and $\{S'_i,S'_{i+1}\} < 2r$.



[Figure 2] An example of complex layout modification for short fault: (a) layout and critical area after layout modification, (b) layout and critical area before layout modification with one bending and (c) layout and critical area after layout modification with two bending.

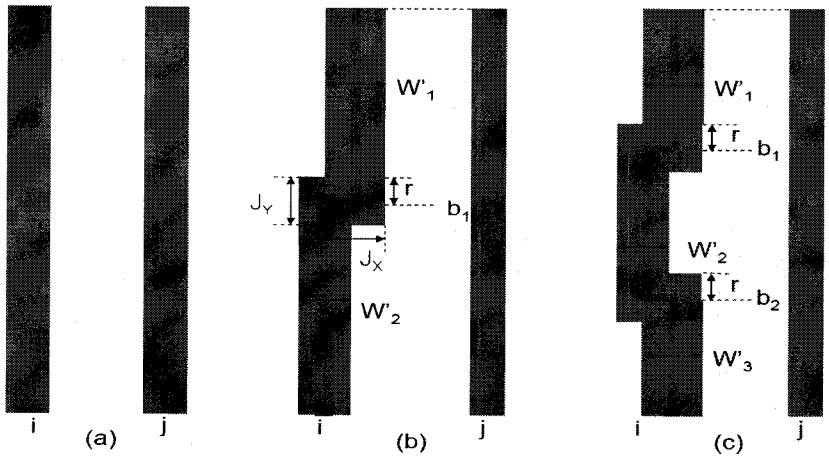
$$DANF(short) = \begin{cases} \int_{S'_i/2}^{max(r)} (S_i - S'_i)L_i D(r)dr + \int_{S'_i/2}^{r} (S_i - S'_i)l(r)D(r)dr + \int_{r}^{L'_{i+1}} (S_{i+1} - S'_{i+1})l(r)D(r)dr & \text{if } S'_i < S'_{i+1}, \\ \int_{S'_{i+1}/2}^{max(r)} (S_{i+1} - S'_{i+1})L_{i+1} D(r)dr + \int_{S'_{i+1}/2}^{r} (S_{i+1} - S'_{i+1})l(r)D(r)dr + \int_{r}^{L'_i} (S_i - S'_i)l(r)D(r)dr & \text{if } S'_i > S'_{i+1}. \end{cases} \quad (7)$$

Here, we assume that S'_i is greater than S_i. Similarly, critical area of Figure 2(c) is divided by three parts of L_1, L_2 and L_3.

For formulation of DANF with respect to open fault, we also generate segments and then calculate critical area for each segment. We can add the critical area caused by jog pattern and thus ANF difference increases if the number of jog increases. We show an example in conditions of $\{W_i,W_{i+1}\} < 2r$, $\{JY_i,JX_i\} < 2r$ and $\{W'_i,W'_{i+1}\} < 2r$ in Figure 3. The yield difference after layout modification is given as equation (9).

$$DANF(open) = \begin{cases} \int_{W'_i/2}^{max(r)} (W_i - W'_i)L_i D(r)dr + \int_{W'_{i+1}/2}^{max(r)} (W_{i+1} - W'_{i+1})L_{i+1} D(r)dr + \int_{JY_i}^{max(r)} (JY_i - 2r)(JX_i - 2r)D(r)dr \end{cases} \quad (8)$$

$$DY = DY(open) * DY(short) = -e^{-ANF(open)}/\Delta ANF(open) * -e^{-ANF(short)}/\Delta ANF(short) \quad (9)$$



[Figure 3] An example of complex layout modification for open fault: (a) layout and critical area before layout modification, (b) layout and critical area after layout modification with one bending and (c) layout and critical area after layout modification with two bending.

3. CONCLUSION AND FUTURE WORK

We propose a novel yield difference in complex layout modification so that yield change is quickly monitored during layout modification, and finally improve critical area robustness and manufacturing yield. This model helps to generate a cost function of defect-limited yield as we device a new layout modification methodology to fix lithography related hotspot.

REFERENCES

[1] G. Allan, "Targeted Layout Modifications for Semiconductor Yield/Reliability Enhancement." IEEE Transactions on Semi. Manufacturing, vol. 17(4), NOV 2004, pp. 573-581.

[2] V. K. R. Chiluvuri, I. Koren, "Layout-synthesis techniques for yield enhancement." 1985, IEEE Transactions on Semi. Manufacturing, vol. 8(2), MAY 1995, pp. 178-187.

[3] J. P. de Gyvez and C. Di, "IC Defect Sensitivity for Footprint-Type Spot Defects." Proc. IEEE Transactions on Computer-Aided Design , vol. 11(5), MAY 1992, pp. 138-158.

[4] W. A. Pleskacz, C. H. Ouyang, and W. Maly, "A DRC-Based Algorithm for Extraction of Critical Areas for Opens in Large VLSI Circuits." Proc. IEEE Transactions on Computer-Aided Design, vol. 18(2), FEB 1999, pp.151-162.

[5] Sean Fitzpatrick, Geoffrey O'Donoghue and Gary Cheek, "A Comparison of Critical Area Analysis Tools", IEEE ISEMI Advanced Semiconductor Manufacturing Conference, 1998, pp. 31-33.

[6] J. Pineda de Gyvez, J. Jess,, "Systematic Extraction of Critical Areas from I.C. Layouts", Defect and Fault Tolerance in VLSI Systems, Ed. C. Stapper, vol. 2, Plenum Press, New York, 1990, pp. 47-61.

[7] http://www.mentor.com

[8] http://www.icyield.com

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