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Max-based Analog Absolute Circuits with Small Error

Maheshwar pd.sah[1], Hai-ping Lin[1], Changju Yang[1], Junho Lee[2] and Hyongsuk Kim[1*]

작은 에러를 갖는 Max 회로 기반 아날로그 절대값 계산 회로

마헤스워 사[1], 임해평[1], 양창주[1], 이준호[2], 김형석[1*]

Abstract Error is the major problem in communication system. Absolute circuit is one of the most important building blocks to implement for the error measurement in communication system as well as in analog circuit design. The main goal of this paper is to design a circuit with high accuracy and minimum error performance. In this paper, a new current mode absolute circuit is implemented to calculate the absolute value of two signals. This new design shows enhanced performance and low distortion over the previous implementation. The proposed circuit is simulated using Hspice and implemented in analog viterbi decoder. It is very suitable for implementing in error calculation for the large scale integrated circuit. Hspice simulation results of previous and new one circuit are reported.

Key Words : current mode, Analog absolute circuit, max-based, small error.

요 약 통신시스템에서의 에러의 처리는 매우 중요한 문제로서 비터비 디코더와 같은 에러처리를 위해서 주로 절대값으로 표현하기 때문에 아날로그 절대값 회로가 자주 필요하게 된다. 이 논문에서는 절대값을 정확하게 계산할 수 있는 아날로그 절대값 회로를 제안하였다. 제안한 절대값 회로에는 부호가 반대인 두 신호들을 만든 다음, 이 신호들을 아날로그MAX회로에 인가하여 둘 중 최대값을 출력하게 하는 방법이다. 이 구조를 회로로 구현하기 위해서는 두 개의 입력 신호를 반대방향으로 차를 구하여, 크기는 같고 부호가 다른 두 개의 신호를 만든 다음 이들을 MAX회로의 입력으로 사용하는 회로를 설계하였다. 본 논문에서는 제안한 회로를 Hspice를 이용하여 시뮬레이션을 수행했으며, 그 결과를 제시하였다.

1. INTRODUCTION

Recently, the absolute circuits are popularly increasing in CMOS analog circuit design. Traditionally most of the analog circuits have been designed in voltage mode [1]. In order to maintain the compatibility with existing voltage processing circuit, current mode circuit has rapid growth in analog circuit design [2]. The use of current mode creates a potential for higher speed, simple structure and low power consumption compared to the voltage mode circuit [3].

The current mode absolute circuits are one of the building blocks and widely used in many applications such as error measurements in communication system, average envelop detector, clock frequency, distant calculation and analog to digital converter [4-5]. However, they are usually required for high performance and low power efficiency with small error. The purpose of this paper is to fulfill the requirements and shows excellent performance which will serve well in increasing need for

[1]Div. of Electronics and Information Eng., Chonbuk National University
[2]Dept. of Mechtronics, Graduate School, Chonbuk National University
[*]Corresponding Author: Hyongsuk Kim(hskim@chonbuk.ac.kr)
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any absolute value of the signal.

The absolute circuit implemented in analog viterbi decoder [6-8] shows inherent error between real and ideal output. In this paper, a new architecture for current mode absolute circuit is presented which features high- precision and high-speed. The paper is organized as follows. In the next section different types of absolute circuits and their operations are described. Section three presents detail operation of proposed circuit. The particular simulation results of different absolute circuits with respect to proposed circuit are discussed in section four. Finally, a conclusionis given in section five.

2. ANALOG ABSOLUTE CIRCUITS

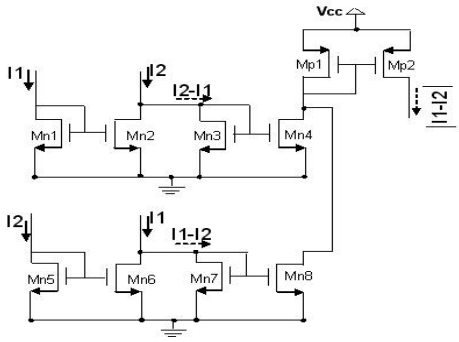
In CMOS technology, several types of analog absolute circuits have been developed for different purpose. The CMOS current mode absolute circuit proposed in analog viterbi decoder [6-8] consist two subtraction and simple addition of these currents as shown in Fig. 1. Two current signals I_1 and I_2 are fed to the upper and lower part of the circuits simultaneously.

The drain current of MOS Mn1 at saturation level is given by

$$I_{ref1} = \frac{1}{2}\mu_n C_{ox}(W/L)_1(V_{GS}-V_T)^2(1+\lambda V_{DS1}) \quad (1)$$

Similarly for Mn2,

$$I_{out1} = \frac{1}{2}\mu_n C_{ox}(W/L)_2(V_{GS}-V_T)^2(1+\lambda V_{DS2}) \quad (2)$$



[Fig. 1] Simple two subtraction absolute circuit.

Generally channel Length modulation λ is zero

$$\frac{I_{out1}}{I_{ref1}} = \frac{(W/L)_2}{(W/L)_1} \quad (3)$$

The output across Mn4 is given by

$$I_{out} = \frac{(W_{Mn4}/L_{Mn4})}{(W_{Mn3}/L_{Mn3})}\left[I_2 - \frac{(W_{Mn2}/L_{Mn2})I_1}{(W_{Mn1}/L_{Mn1})}\right] for\ I_2 > I_1$$

$$= 0 \qquad for\ I_2 \le I_1 \quad (4)$$

If the aspects ratios (W/L) of upper and lower are same

$$I_{out} = I_2 - I_1 \quad for\ I_2 > I_1$$

$$= 0 \qquad for\ I_1 \le I_2 \quad (5)$$

Similarly for the lower part of the circuit, the current at Mn8 is,

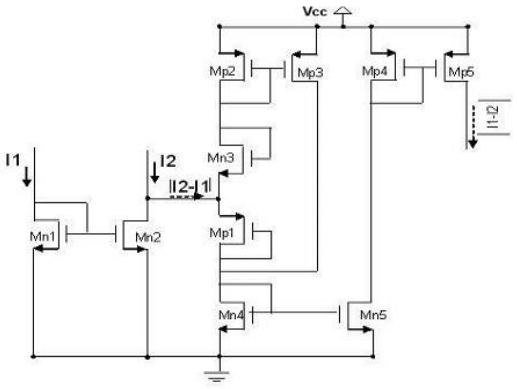
$$I_{out} = I_1 - I_2 \quad for\ I_1 > I_2$$

$$= 0 \qquad for\ I_1 \le I_2 \quad (6)$$

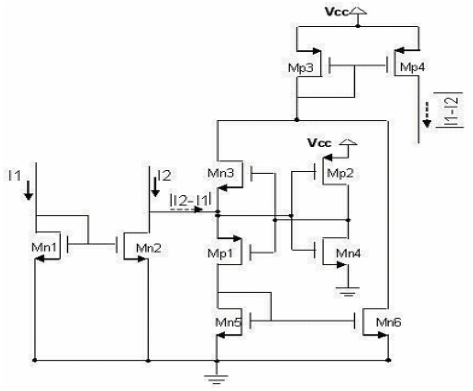
When $I_1 > I_2$, the drain voltage of Mn2 drops quickly so that Mn4 becomes cut off. Meanwhile, the current (I_1-I_2) obtained at the lower part of the circuit is fed into the diode connected circuit of Mn7. In the end, the current mirror Mn8 produces I_1-I_2. The current is copied by another current mirror Mp1 and Mp2. When $I_2 > I_1$, Mn8 is cut off and I_2-I_1 obtained from the upper part of the circuit.

The major drawback of this approach is at the zero crossing of the two input currents or when $I_1 = I_2$. The current at the drain terminal of Mn2 and Mn6 become zero. Therefore, the voltage at this point is also zero. In this moment Vd<Vg>Vs which shows the MOSFET temporarily in the triode region instead of cut off mode. So the circuit creates maximum error compare to the ideal output of absolute current (I_1-I_2). The circuit can not operate at high frequency mode due to high output impedance.

Another solution for increasing the performance at the zero crossing of the current signal is a simple full wave current rectifier.



[Fig. 2] Current rectification based absolute Circuit.



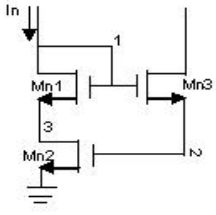
[Fig. 3] Comparator based absolute circuit.

circuit with diode connected MOSFETS as shown in Fig. 2. Here Mp1 and Mn3 are equivalent of two diodes connected with opposite polarity. When $(I_2-I_1) > 0$, Mp1 will forward bias and current flows across Mn4 which is copied to Mn5. The operation is reversed when $(I_2-I_1) < 0$, Mn3 will forward bias and current flows across Mp2 to Mp3. Therefore, the total output across Mp5 is absolute value of (I_1-I_2). The performance of the real output is better than previous circuit and nearly same as ideal. One of the problems associated in this circuit is the inherent error after completion of one cycle. In each cycle of operation either Mn3 or Mp2 should be cut off while other is in saturation but temporally one MOS is always in triode region which tends to maximum error and feed back highly distortion in the input signal.

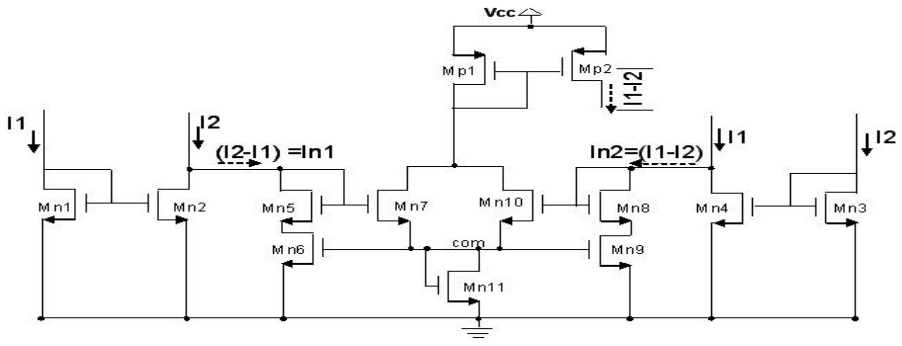
The distortion in the input signal can be modified using a simple comparator circuit [9-10]. It is based on subtraction (Mn1, Mn2) and comparator (Mn3, Mp1, Mp2, Mn4) as shown in Fig. 3. It has input impedance rPMOS//rNMOS. The input state of this architecture has source follower which introduces feed back into the gates. A positive feedback from an inverter is used to achieve enough gain to amplify small voltage variation in the input stage node [15]. When $(I_2-I_1)>0$ or $I_2>I_1$, the source follower of Mp1 and Mn3 are forward and reverse bias respectively. Simultaneously the inverter of Mn4 turns on, so the drain voltage of this MOS will low.

The feedback across the drain of Mn4 turns on the MOS Mp1 and (I_2-I_1) obtained across Mn5. The current is copied by current mirror Mn6. The situation is reversed when $(I_2-I_1) < 0$ or $(I_2<I_1)$, Mn3 will forward bias and the inverter of Mp2 turns on. The drain voltage of this MOS is high, so the feedback of the inverter turns on Mn3 and (I_1-I_2) is obtained across Mp3 to Mp4. Therefore, the total output current across Mp4 is absolute value of (I_1-I_2). The circuit however shows deadband region for dynamic response of small input current in which the two input transistors are turned off temporarily [16]. At this time the input resistance is quite high and thus limiting the speed of operation and some delay between the real and ideal output of the current signal [18].

In this paper, a new CMOS current absolute circuit is proposed which takes advantages such as simple structure, low power consumption and low distortion compared to above circuits. Hspice is used to verify the simulation result of the circuit.



[Fig. 4] Basic cell of max circuit.



[Fig. 5] Proposed max based absolute circuit.

3. PROPOSED CIRCUIT

With the increasing popularity in analog absolute circuits design several approaches have been reported. From this discussion, it is noted that there is still necessary to improve performance of the circuits. One of the absolute circuit proposed in this is research is based on the simple operation of subtraction and max [8]. The max circuit was selected because it shows excellent performance to select max output among different current signals and overcome the problems encounter in above circuits [11]. Fig. 4 illustrates the basic cell of the max circuit. It is based on simple operation and cascade connection of various circuits. The node voltage 2 is associated with maximum input currents following in the circuits and it decides the saturation mode of the Mn2. At the same moment voltage at node 2 is copied to node 3 so the saturation of Mn1 and Mn3 also depend on this voltage. This is how the node voltage 2 controls all the MOS in saturation region. The basic diagram of proposed absolute circuit is shown in Fig. 5. The MOSFETS (Mn1, Mn2) and (Mn3, Mn4) compose the subtraction of two current signals (I_2-I_1) and (I_1-I_2) respectively. Other parts are the basic cells of max circuit for two inputs currents. Mn11 is the diode connected transistor for a current source act as winner transistor that is I_{max} [12].

Let In_1= (I_2-I_1) and In_2= (I_1-I_2).

When In_1 > In_2, the voltage at node **com** is associated with In_1, as a result this node voltage controls the Mn5, Mn6 and Mn7 in saturation mode. The current In_2 will flow through Mn9 such that the drain voltage of Mn9 drops abruptly and so the source and gate voltage of Mn8 which results in that Mn10 becomes cut off. Thus, the maximum current In_1 flows only through Mn7 which appears at the output.

On the other hand, incase In_2>In_1, Mn7 is cut off and the current flowing through Mn10 equals to In_2. Following is the summary of such operation

I_{out} = Max (In_1, In_2)
= Max ((I_2-I_1), (I_1-I_2)) = |I_1-I_2|

4. SIMULATION RESULTS

Hspice is used to verify the simulation result of the proposed circuit using standard 0.18μm CMOS process with 3.3V power supply. The transistors aspect ratio of proposed circuit is summarized in Table1. All the transistors and current mirrors were designed approximately to minimize the parasitic capacitance and mismatch effects. Since we are considering current mode of circuit, the voltage is converted to current mode by voltage to current converter (V to I) [8]. Two sinusoidal voltages 1.65V at the frequency 40 MHz and 50 MHz are converted to current mode using V to I circuit. The corresponding output currents are shown in Fig. 6.

When the two input currents are equal, the amplitude of the ideal output is zero, generally known as minimum point and when the difference is high, the amplitude is maximum called the maximum point.

Fig. 7(a) is the simulation and experimental output waveform of the subtraction based absolute circuit. The dash and bold line represent the real and ideal output of absolute current (I1-I2) respectively.

[Table 1] Transistors aspects ratio dimension

Transistors	W($\mu\mu$m)	L($\mu\mu$m)
Mn1,Mn2,Mn3,Mn4,Mn6,Mn1Mn9	12	0.4
Mn5,Mn7,Mn10,Mn8	4	0.4
Mp1,Mp2	8	0.4

The difference between real and ideal output measured in minimum and maximum points are approximately 60% and 26.27% respectively. The average error between these two points is 43.27% which shows maximum error in the circuit. The circuit consists only two subtraction parts. It consumes a certain amount of power and the parasitic capacitance associate in the MOSFETS result closely 1.2nsec time delay between real and ideal output.

Fig. 7(b) is the output waveform of the current rectifier based absolute circuit. The errors measured at minimum and maximum points are nearly 9.03% and 7.22% respectively. The average error and time delay measured in this circuit is approximately 8.13% and 1.4nsec respectively. The subtraction parts associated in the circuit and only one operation of MOSFET in each cycle of input signal performs a little bit more time delay compare to the real and ideal output. The results show a big progress compare to previous circuit. However, the error is still high.

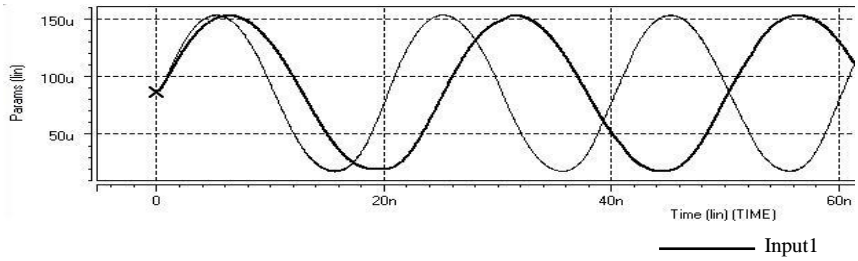
Fig.7(c) is the real and ideal output of the comparator based absolute circuit. It shows errors at minimum and maximum points are nearly 3.03% and 6.67% respectively with average error 4.85%. The time delay between real and ideal output is close to 1.5nsec. The average error is reduced. However, the temporarily deadband region for the small input currents, the output resistance is high, time delay and limits the speed [16-18].

Fig. 7(d) is the simulation result of the proposed circuit. It shows 1.27% and 1.53% errors at minimum and maximum points and nearly 1.5nsec time delay. The mismatch and internal parasitic capacitance of the substractor and max circuit result a time delay between real and ideal output. The average error of 1.40% between real and ideal output confirms an excellent progress of the circuit.

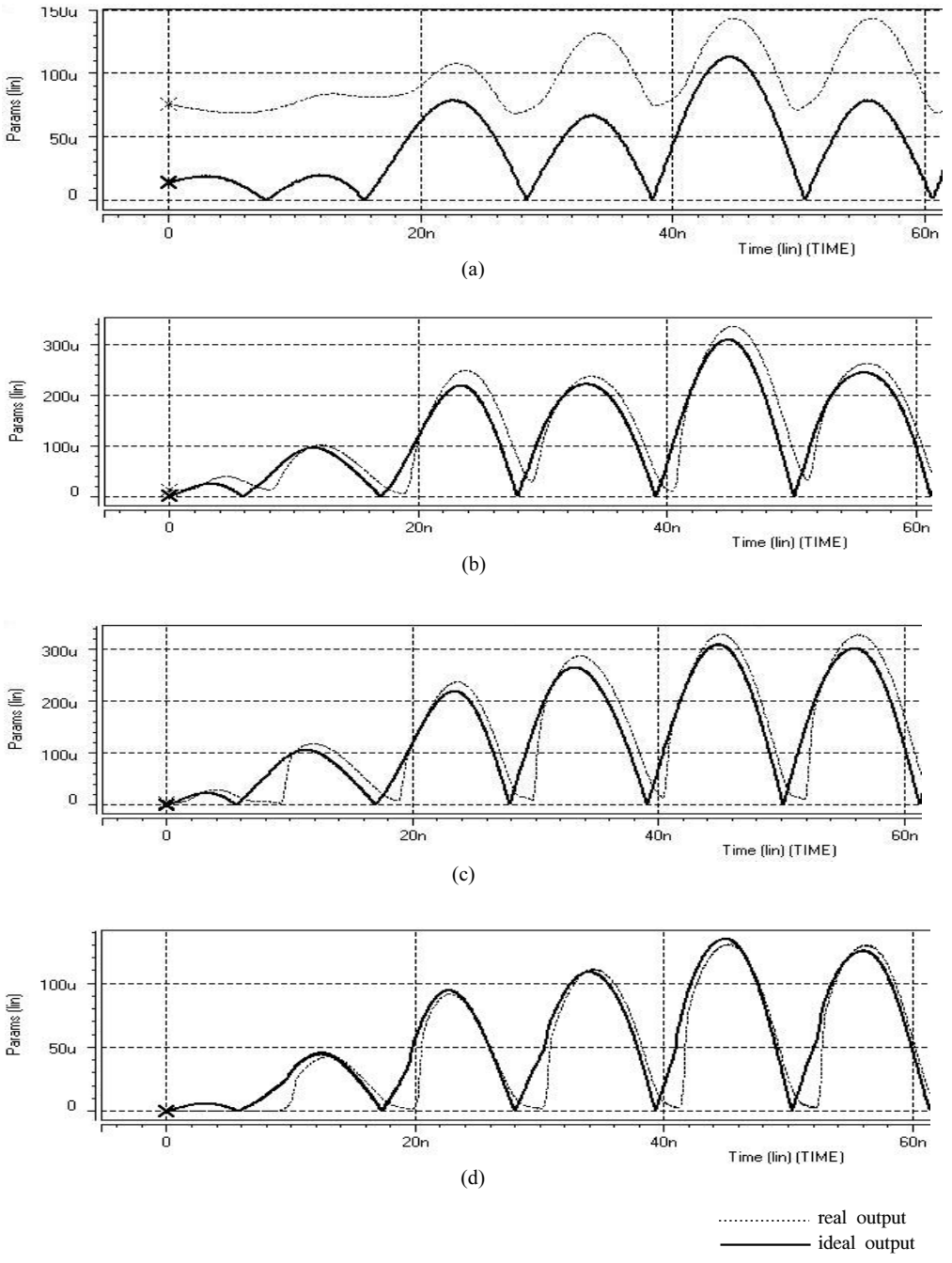
The power dissipation, speed of operation and power delay product are too optimistic as subtraction circuit also consumes certain amount of power and exhibits certain delay time [18]. So all the circuits present in this paper show little bit delay with real and ideal output as absolute circuits consist subtraction of current signal. The comparison results of the circuits are summarized in Table 2.

5. CONCLUSION

In analog absolute circuit, the circuit is designed to achieve the output performance as the exact replica of the ideal signal, so that error can be reduced in the minimum level. In this paper, we discuss simulation results of different absolute circuits. The proposed circuit only shows the real output is exact mimic of the ideal. Though, it has little more delay but the quality of real output is excellent and nearly close to ideal. The new circuit is an accurate and one of the most challenging in the circuit design. The summarized results of different circuit presented in Table 2 shows the purposed has the least error in comparison with real and ideal output among others. The most important issue in this paper is that the output performance is better and great improvement with high accuracy even in the high frequencies of the input signals. This change represents, it is one of the most promising circuit which can work well and suitable for implementing in analog circuit design to calculate the absolute value of current or error in communication system.



[Fig. 6] Input waveform.



[Fig. 7] Output waveform of the absolute circuits:
(a) Two subtraction based (b) Current rectifier based (c) Comparator based (d) Max based.

[Table 2] Comparison results

S.n	Circuits	Time delay (n sec)	Maximum % error at minimum point	Maximum % error at maximum point	Average % error
1	Two Subtraction absolute circuit	1.2	60	26.54	43.27
2	Full wave rectification based absolute circuit	1.4	9.03	7.22	8.13
3	Comparator based absolute circuit	1.5	3.03	6.67	4.85
4	Max based absolute circuit	1.5	1.27	1.53	1.40

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Maheshwar Prasad sah [Regular Member]

- Aug. 2005: Pokhara University Nepal Electronics and Communication Engineering
- Mar. 2008 : Div. of Electronics and Information Eng., Chonbuk National University (Master student)

<Research Interests>
Integrated Circuits Design and implementation of error correction circuits, Robot Vision

Haiping Lin [Regular Member]

- July 2005 : South-central-University for Nationalities, China
- Sept. 2007: Div. of Electronics and Information Eng., Chonbuk National University, MS
- Aug. 2007 : Div. of Electronics and Information Eng., Chonbuk National University, PhD student

<Research Interests>
Robotvision, Analog Parallel Processing Circuits

Changju Yang [Regular Member]

- Feb. 2008 : Div. of Electronics and Information Eng., Chonbuk National University, BS
- Mar. 2008 : Div. of Electronics and Information Eng., Chonbuk National University, Master Student

<Research Interests>
Analog Integrated Circuits, CNN, Robot Vision

Junho Lee [Regular Member]

- Feb. 1998 : Dept. of Mechanical Eng., BS
- Feb. 2000 : Dept. of Mechanical Eng, Wonkwang U., MS
- Mar. 2004 ~ Present : Dept. of Mechatronics Eng. PhD student
- 2007 ~ Present : JinWoo SMC CEO

<Research Interests>
Optimal design of oil pressure, Robot Vision

Hyongsuk Kim [Regular Member]

- Jan. 1982~Aug. 1992: Senior Researcher, Agency for Defense Development
- May 1992 : University of Missouri, Columbia, PhD.
- September 1993 ~ present: Professor, Div. of Electronics and Information Eng., Chonbuk National University

<Research Interests>
Robot Vision. Sensors of Robots, Analog Parallel Processing System