Advanced SOI LDMOS Incorporating Multiple Trench Oxide Structures for Enhanced Breakdown Voltage

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항복 전압 향상을 위한 다중 트렌치 산화막 구조 기반의 고성능 SOI LDMOS

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Abstract

A new lateral double diffused MOSFET (LDMOS) on a silicon substrate with a multiple trench oxide structure (MTS) embedded under the field oxide in the drift region is presented. The MTS is introduced to mitigate electric field crowding at the drain edge, which is the primary factor limiting breakdown performance in conventional racetrack source (STD) LDMOS devices. Devices were fabricated using a CMOS compatible process flow and systematically characterized. Experimental results demonstrate that the proposed MTS LDMOS achieves up to a 40% enhancement in drain to source breakdown voltage (BVdss) compared with the STD counterpart at a drift length of 25μm, while maintaining acceptable conduction characteristics. The proposed structure offers a simple yet effective approach to improving the high voltage capability of LDMOS devices for advanced power management ICs.

1. Introduction

Lateral double diffused MOSFETs (LDMOSFETs) are widely deployed in high voltage integrated circuits due to their process compatibility with CMOS technology, high input impedance, and straightforward integration with control circuitry[1,2]. In applications such as power management ICs, motor drivers, and telecommuni-cation line drivers, LDMOS devices enable monolithic integration of low voltage logic with high voltage switching elements.

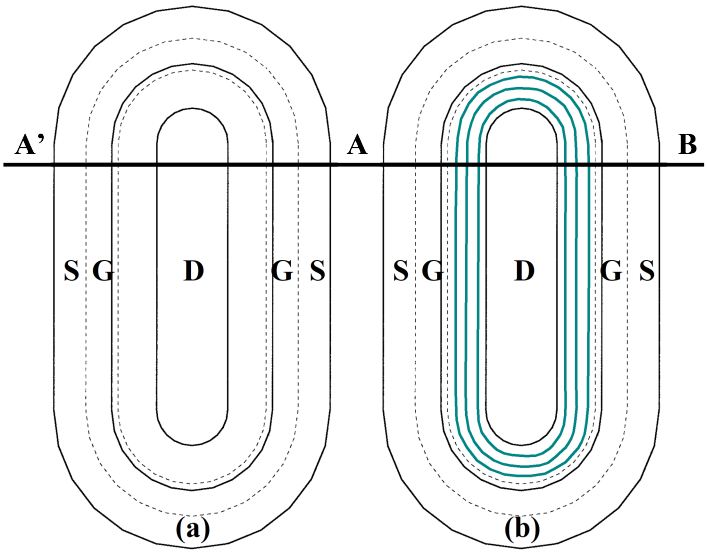
However, standard racetrack source LDMOS devices are constrained by limited breakdown voltage. The rounded drain geometry leads to localized electric field crowding, current crowding, and localized self-heating, all of which reduce BVdss and device reliability. Several methods have been reported to address this challenge, including the use of multiple floating guard rings, RESURF techniques, and deep p-top implants[3,4]. These approaches, while effective, increase process complexity and design overhead.

This work proposes a multiple trench oxide structure (MTS) beneath the field oxide of the drift region as an alternative solution. The MTS acts as an effective field relief mechanism, redistributing the electric field and reducing its peak value near the drain edge. Unlike more elaborate techniques, this approach requires minimal deviation from standard CMOS processing, making it attractive for manufacturable high voltage device design.

2. Experiment

2.1 Device Structure

Two device types were investigated: (i) a standard racetrack source LDMOS (STD) and (ii) the proposed multiple trench oxide structure LDMOS (MTS). The MTS device incorporates vertically etched oxide filled trenches under the drift region field oxide, as opposed to the uniform LOCOS oxide of the STD device (Fig. 1).

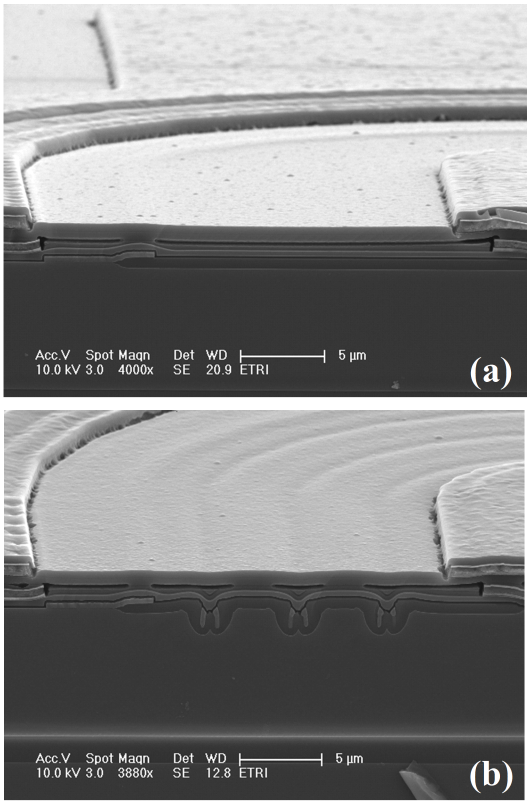


[Fig. 1] Schematic diagram of n-LDMOSFETs with different field structures: (a) STD, (b) MTS.

2.2 Fabrication Process

Fabrication was performed on SOI wafers with a 3 μm buried oxide and an 8.5 μm lightly doped p-type top silicon layer (~1×10^{15} cm^{-3}). After deep n-well formation, multiple trenches were etched by reactive ion etching (RIE) using a CCl_4 + O_2 gas mixture. A phosphorus implant (~2×10^{12} cm^{-2}) defined the auxiliary n-drift region, and a boron implant formed the high voltage p-well, followed by high temperature annealing at 1150 °C in N_2 ambient.

Field isolation was achieved using a 7000 Å LOCOS oxide. Threshold voltage adjustment was performed via BF_2 implantation. Gate oxides of 350 Å (LDMOS) and 200 Å (CMOS) were thermally grown. 3800 Å-thick polysilicon gate electrode was deposited by LPCVD and doped in $POCl_3$. After gate patterning, source and drain regions were implanted (As for N^+, BF_2 for P^+) and annealed at 950 °C. The devices were completed using conventional CMOS metallization. SEM images of fabricated structures are shown in Fig. 2.



[Fig. 2] SEM cross-sectional photographs of fabricated devices: (a) STD, (b) MTS.

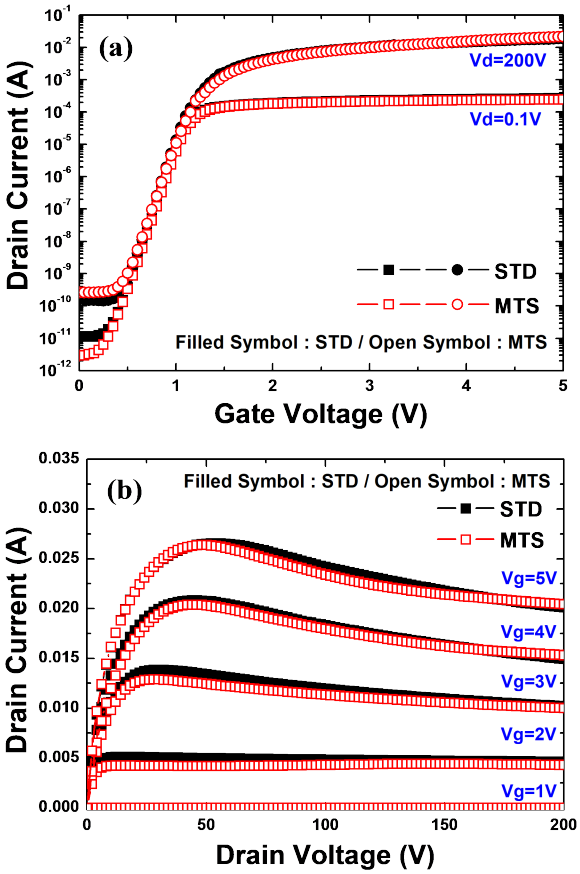
2.3 Characterization

Electrical characterization was carried out at 298 K using an HP4156B semiconductor parameter analyzer and a Tektronix 370A curve tracer. Breakdown voltage was measured under off state conditions (V_{GS} = 0 V).

3. Results and Discussion

3.1 Forward Conduction

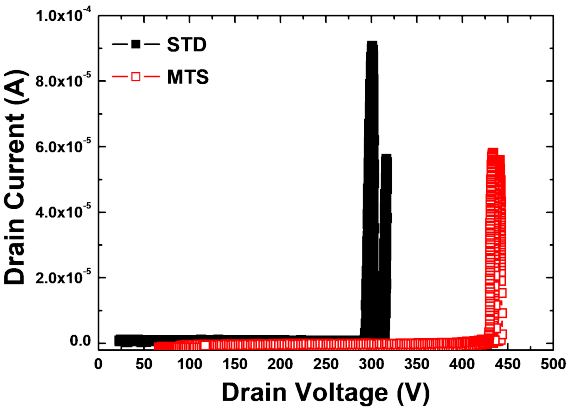
Figure 3 shows the forward conduction characteristics of the STD and MTS devices. The MTS device exhibits slightly reduced linear current (~9%) compared with the STD design, attributed to lower effective field in the drift region. Nevertheless, the reduction in self heating due to improved current distribution compensates for this drawback.



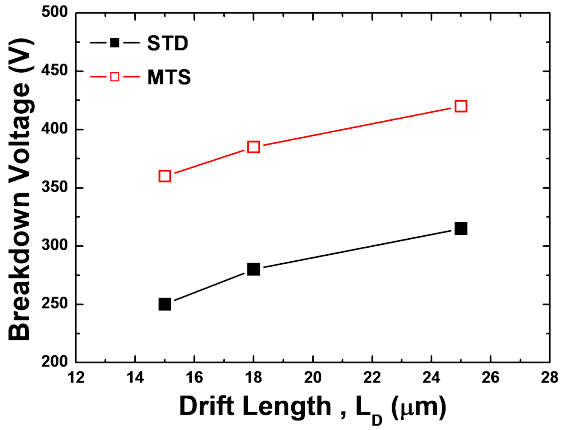
[Fig. 3] Forward conduction characteristics: (a) I_{DS}-V_{GS} at V_{DS} = 200 V, (b) I_{DS}-V_{DS} at various V_{GS}.

3.2 Breakdown Voltage

The I_{DS}-V_{DS} characteristics at V_{GS} = 0 V (Fig. 4) highlight the significant enhancement in BVdss with the MTS design. At a drift length of 25 μm, the MTS device achieved ~40% higher BV_{dss} compared with the STD device. Figure 5 summarizes BV_{dss} scaling with drift length: the MTS consistently outperformed the STD structure across all tested lengths, confirming the scalability of the approach.



[Fig. 4] Off-state drain current vs. drain voltage showing breakdown characteristics at L_D = 25 μm.



[Fig. 5] BVdss as a function of drift length for STD and MTS devices.

The superior breakdown performance is attributed to the field relief function of the oxide trenches, which suppresses peak field concentration at the drain edge[5,6]. This reduces localized avalanche generation and delays the onset of breakdown. Furthermore, the trenches mitigate current crowding, thereby alleviating localized heating effects.

3. Conclusion

A new n-LDMOS with multiple trench oxide structures embedded beneath the driftregion field oxide has been fabricated and experimentally validated. The MTS LDMOS exhibits a significant improvement in breakdown voltage up to 40% higher than that of conventional racetrack source devices while maintaining reasonable conduction performance. This CMOS compatible structural modification provides a practical and manufactur-able solution for enhancing high voltage robust-ness of LDMOS transistors, making it suitable for next generation power management IC applications.

References

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