High Reliability Trench-Gate Power MOSFET with Stacked Gate Oxide Structure for Electric Vehicle Applications

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전기차 적용을 위한 적층 게이트 산화막 구조를 이용한 고신뢰성 트렌치 게이트 파워 MOSFET

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Abstract

In this paper, we propose a stacked structure of gate dielectrics to suppress of hump phenomena and to improve gate oxide reliability in trench-gated power MOSFETs with a gate oxide thickness of 700 Å. In case of stacked-dielectric structure formed by thermal oxidation and subsequent chemical vapor deposition (CVD), no hump phenomena is shown contrary to only thermal oxide (SiO_2) case. Furthermore, reliability characteristics are dramatically improved by the stacked structure with low gate leakage current and high breakdown voltage even in larger cell size, whereas in case of only thermal oxide they become worse for greater cell size. These improvements are due to the excellent uniformity of gate oxide thickness at the trench bottom corner region.

1. Introduction

Power metal oxide semiconductor field effect transistor (MOSFETs) have been widely adopted in various applications such as automatic electronics, wireless communication, etc [1-4]. One of the popular device structures in automotive application is trench gate power MOSFETs, which requires high current driving capability to reduce power consumption and to increase switching speed [5,6]. Generally, the trench gate structure allows greater current drivability, higher package density and lower on-state resistance than planar devices because gate and source are located at the wafer surface and the drain is located at the back side of wafers. The issues in trench gate power MOSFETs, such as, hump phenomena and reliability characteristic are of concern due to the thinning of local oxide thickness induced by various surface orientations at the trench surfaces. The degradations of hump phenomena and reliability occur due to the concentrated high electric field at the thinner gate oxide around the trench edges [7-9]. To prevent the localized oxide thinning, various process and technique have been proposed. For example, high-temperature oxidation process or chemical dry etching (CDE) process applied effective method for rounding off the trench edges. However, reliability characteristics of trench gate oxide formed by these techniques were insufficient for devices with high density trench gate [10]. On the other hand, it has been reported that the reliability immunity of a capacitor can be improved by CVD film which is known to be suitable for the planar high voltage MOSFETs. Although the CVD film can also be used for the trench gate dielectric, the reliability issue can be still a concern.

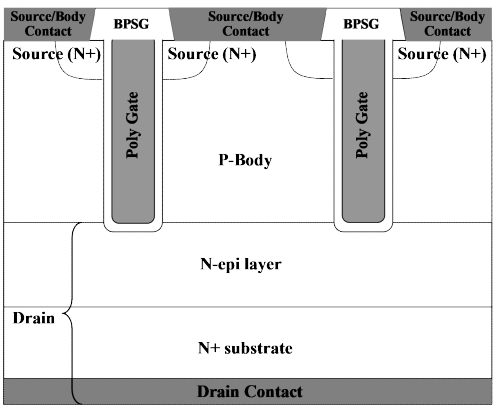
In this work, a novel stacked gate dielectric structure is proposed to improve the reliability as well as to suppress the hump phenomena for high density trench gate power MOSFETs.

2. Experiment

A phosphorus-doped epitaxial Si layer was epitaxially grown on heavily doped n-type Si (100) substrate. In order to protect the surface

during the grooving or silicon etching, wafer was slightly oxidized to a thickness of 400 Å. Then, after boron implantation to form the body region, rectangular grooves with a depth of 2.0 μm were formed by relative ion etching (RIE) using a gas mixture of $CC1_4$ + O_2. The surface of the grooves was slightly etched off in saturated ammonium hydroxide at a temperature of 90 °C. Next two kinds of gate oxide i.e. thermal SiO_2 and thermal SiO_2+CVD oxide are applied. 700 Å and 250 Å-thick gate oxides were thermal grown in O_2 ambient at 1100 °C and 450 Å-thick CVD oxide is deposited only on the 250 Å-thick gate oxide. Polysilicon was deposited by LPCVD with $POCl_3$ doping in N_2/O_2 ambient at 875 °C and patterned so that only the trench area could be covered by polysilicon. Then, arsenic ions were implanted and annealed to make source region with a 0.4 μm depth. The trench gate power MOSFETs structure is illustrated in Fig. 1. Power MOSFETs with only 700 Å-thick thermal oxide is named as 'Thermal Oxide' and that with 250 Å-thick thermal oxide and 450 Å-thick CVD oxide is named as 'Stacked Oxide' in short, respectively.

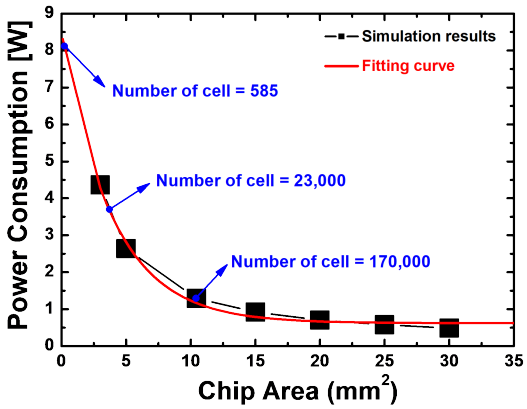
The electrical characteristics of the trench gate MOSFETs were measured at room temperature (298K) using an Agilent 4156B semiconductor parameter analyzer, Tektronix 370A curve tracer and a semi-automatic shielding prober.



[Fig. 1] Illustration of device structure of trench gate power MOSFETs.

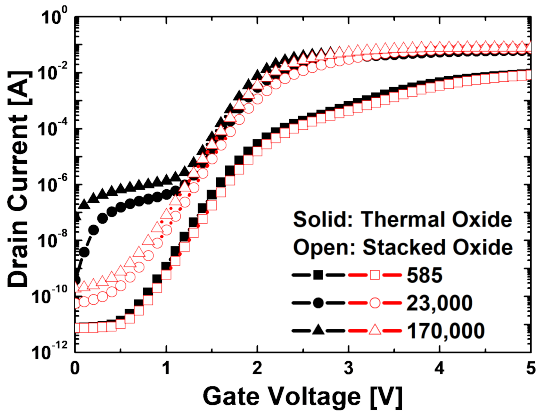
3. Results and Discussion

Figures 2 show after 10,000 s stress, the STD device showed severe degradation (gm,max ↓22.5% Figure 2 shows simulation results of power consumption as a function of chip area in trench gate power MOSFETs. Power device needs to have larger cell density because the power consumption decreases as the chip area increases.



[Fig. 2] Simulation results of power consumption as a function of chip area. i.e., number of cell.

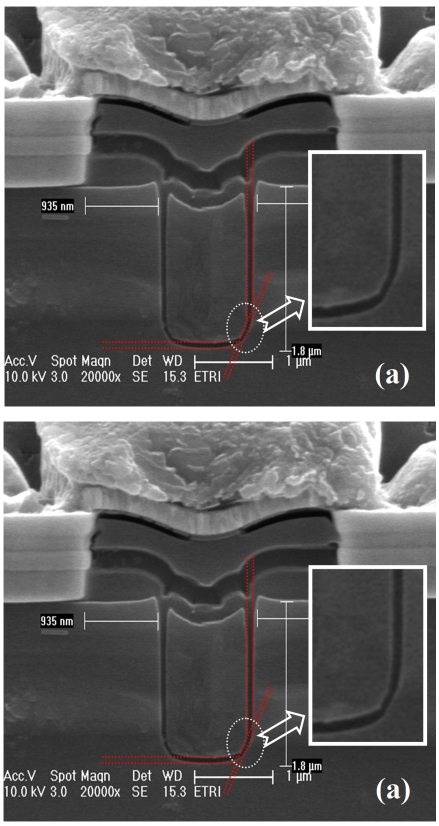
However, greater cell density can increase the possibility of the formation of locally thin gate oxide especially at the trench bottom corner region. I_D-V_G characteristics are monitored for various cell density to clarify the dependence of device performance on the cell density as shown in Fig. 3.



[Fig. 3] I_D-V_G characteristics of power MOSFETs under positive and negative gate bias condition.

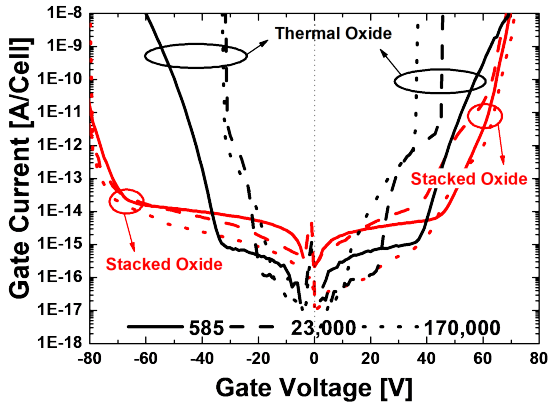
In case of Thermal Oxide, subthreshold hump phenomena is monitored in high density (23,000 ea and 170,000 ea) power MOSFETs, while no hump happens in lower density (585 ea) power MOSFETs. That is, hump phenomena increases as the cell density increases because non-uniformity of trench gate thickness induced by gate oxide thinning increases as the cell

density increases. These hump phenomena can be explained by a general recess hump model [11,12], which is due to the electric field (E-field) crowding effect by the gate oxide thinning at the trench corner region as shown in Fig. 4(a). However, in case of Stacked Oxide, no hump characteristic is monitored contrary to Thermal Oxide case as shown in Fig. 3. These result can be supported by cross-sectional SEM image of fabricated devices as shown in Fig. 4 (a) and (b). Oxide thickness at the trench edge region of Stacked Oxide and Thermal Oxide is 68 nm and 58 nm, respectively. That is, Stacked Oxide has little thinning of gate oxide due to the little dependence of LPCVD oxide thickness on the trench geography. Therefore, stacked dielectric structure can be a good candidate for high performance trench gate power MOSFETs without hump phenomena.



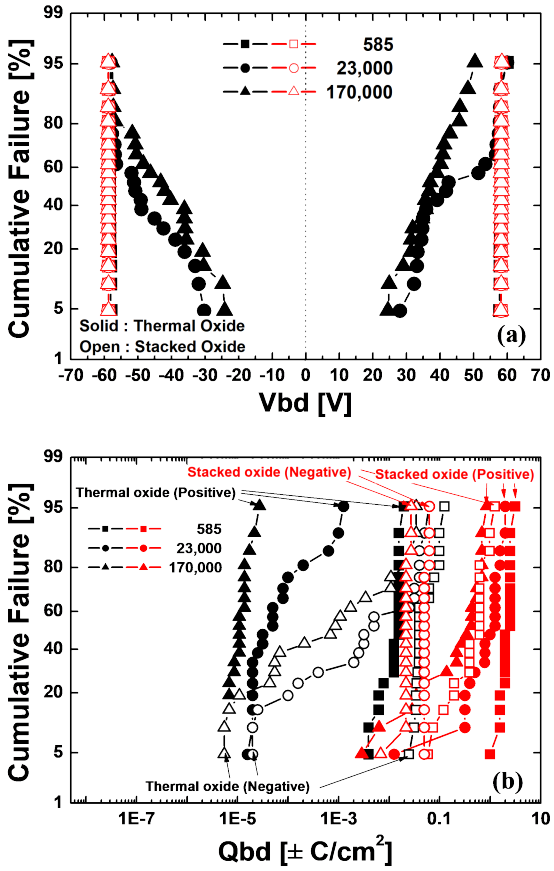
[Fig. 4] Cross-sectional SEM images of (a) Thermal Oxide and (b) Stacked Oxide. The Stacked Oxide shows uniform oxide thickness at the trench bottom corner region.

Reliability as well as DC characteristics should be considered for development of power MOSFET. Therefore, breakdown characteristics are monitored as a function of cell density as shown in Fig. 5. Although gate leakage current density (J_G) of Stacked Oxide is larger than that of Thermal Oxide at low Vg region, J_G of Thermal Oxide case exhibits great increase at high V_G region while that of Stacked Oxide shows low level for wide gate voltages. Stacked Oxide shows small leakage current and higher intrinsic breakdown voltage for all cell densities as well as all bias conditions that is both in inversion and accumulation regions.



[Fig. 5] Comparison of I_G-V_G characteristics between Thermal Oxide and Stacked Oxide 소드믹malr ion on niform viate at 23000 ea case while stacked structure shwo under positive and negative gate bias conditions.

Fig. 6 (a) shows cumulative probability of breakdown voltage(V_{bd}) under gate injection (negative) and substrate injection (positive) conditions. V_{bd} distribution of minimum size cell (585 ea) shows same breakdown voltage between the two structures. However, the distribution of breakdown voltage of Thermal Oxide begins to deviate at 23000 ea case while Stacked Oxide shows uniform distribution for all cell size. Moreover, Q_{bd} distribution shows same tendency with V_{bd} distribution as shown in Fig 6. (b).



[Fig. 6] Comparison of (a) breakdown voltage, V_{bd} and (b) charge to breakdown, Q_{bd} cumulative probability between two gate oxide structures.

3. Conclusion

Trench gate power MOSFETs with a novel stacked oxide is proposed to suppress hump phenomena and to improve gate oxide reliability. The proposed power MOSFETs with the Stacked Oxide exhibited no hump phenomena for all cell density while power MOSFETs with only thermal oxide had a dependence of hump phenomena on the cell density. Moreover, the stacked oxide case exhibited stable distributions of breakdown voltage and charge-to-breakdown. The superior performance of stacked gate oxide to conventional thermal oxide only case is due to the formation of uniform oxide thickness at the trench bottom corner. Therefore, the proposed stacked gate oxide structure is highly promising for high performance trench gate power MOSFETs.

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