Hot Carrier Reliability Improvement in n-LDMOS through Multiple Trench Oxide Structures

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다중 트렌치 산화막 구조 적용에 따른 n-LDMOS의 핫 캐리어 신뢰성 개선

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Abstract

The impact of multiple trench oxide structures (MTS) on the hot carrier (HC) reliability of n-channel lateral double diffused MOSFETs (n-LDMOS) fabricated on SOI substrates is investigated. Devices with and without the MTS were subjected to long term electrical stress at VGS=5 V and VDS=200 V for up to 100,000 s. The standard racetrack source (STD) LDMOS exhibited substantial degradation, including a 22.5% reduction in maximum transconductance and a 2.3% increase in threshold voltage after 10,000 s. In contrast, the MTS device demonstrated only 2.5% transconductance degradation and a negligible 0.5% threshold voltage shift under identical stress. In addition, the MTS device showed superior immunity to drain current and on resistance degradation. These results confirm that the MTS effectively suppresses hot carrier induced damage and greatly enhances device reliability, complementing its previously reported breakdown voltage benefits.

1. Introduction

Reliability is a key concern for high voltage MOSFETs in power management and mixed signal ICs. Among various degradation mechanisms, hot carrier effects are particularly detrimental to LDMOS transistors, as they are typically operated under large drain to source voltages. Hot carriers generated near the drain edge can be injected into the gate oxide, resulting in trapped charges, interface trap creation, and mobility degradation. These effects manifest as threshold voltage shifts, transconductance degradation, and increased on resistance[1].

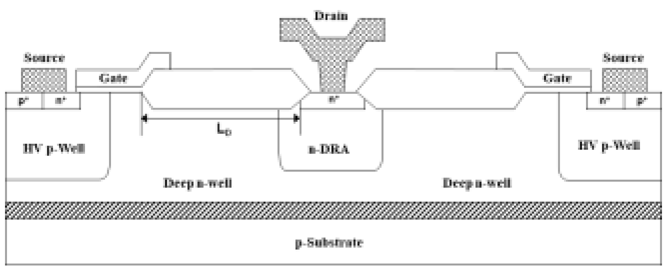
Standard racetrack source LDMOS devices are highly susceptible to HC degradation due to electric-field concentration at the drain edge. Previous studies have proposed process modifications such as RESURF or deep p-top implants; however, these methods add design and process complexity. Recently, the multiple trench oxide structure has been proposed as a means to enhance breakdown voltage by reducing peak field intensity.

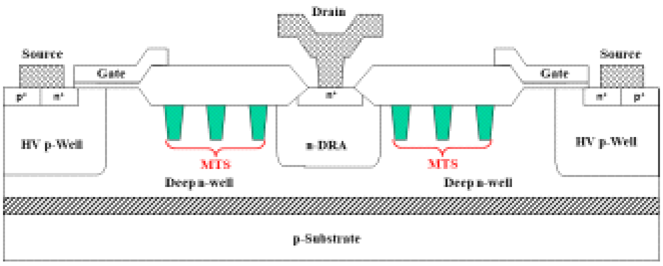
In this paper, we demonstrate that the same mechanism also significantly improves HC reliability.

2. Experiment

2.1 Device Structure

Two device types were investigated: (i) a standard racetrack source LDMOS (STD) and (ii) the proposed multiple trench oxide structure LDMOS (MTS). The MTS device incorporates vertically etched oxide filled trenches under the drift region field oxide, as opposed to the uniform LOCOS oxide of the STD device (Fig. 1).





[Fig. 1] Cross-sectional views of n-LDMOSFETs along cut lines (a) STD and (b) MTS.

2.2 Stress Conditions

Devices were stressed at VGS = 5 V and VDS = 200 V for durations up to 100,000 s at room temperature. IDS -VGS and gm-VGS characteristics were measured before stress and at regular intervals using an HP4156B analyzer. Threshold voltage was extracted using the linear extrapolation method at VDS = 100 mV.

2.3 Evaluation Metrics

The following reliability indicators were assessed:

1) Degradation in maximum transconductance (gm,max)
2) Threshold voltage shift (ΔVt)
3) Drain current reduction (ΔIDS)
4) On-resistance increase (ΔRon)

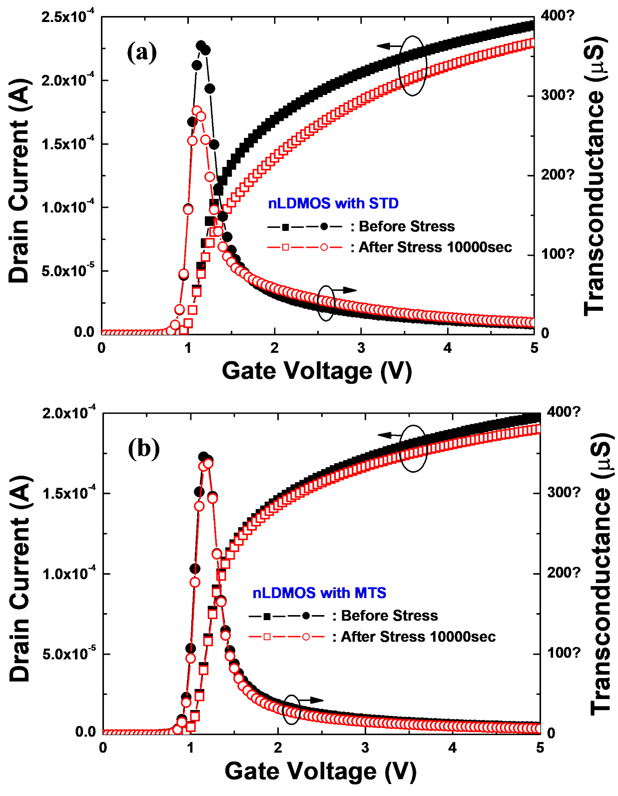
2.3 Characterization

Electrical characterization was carried out at 298 K using an HP4156B semiconductor parameter analyzer and a Tektronix 370A curve tracer. Breakdown voltage was measured under off state conditions (VGS = 0 V).

3. Results and Discussion

3.1 Transconductance and Threshold Voltage

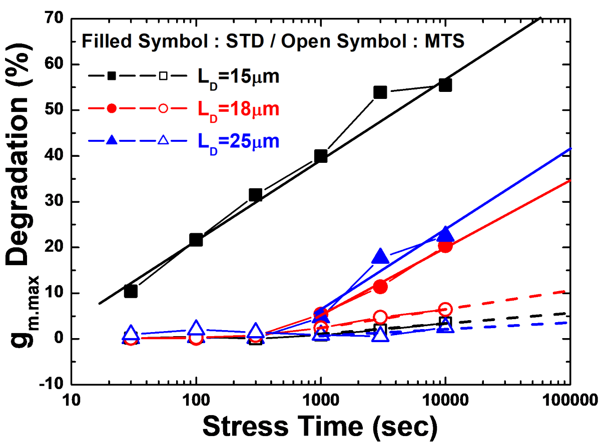
Figures 2 show after 10,000 s stress, the STD device showed severe degradation (gm,max ↓22.5%, Vt ↑2.3%). In comparison, the MTS device degraded only slightly (gm,max ↓2.5%, Vt ↑0.5%). These results confirm that MTS effectively suppresses HC induced trap generation and interface state formation at the drain side gate edge[2-8].



[Fig. 2] $I_{DS}-V_{GS}$ characteristics of n-LDMOSFET before and after hot carrier stress, (a) STD and (b) MTS.

3.2 Drift Length Dependence

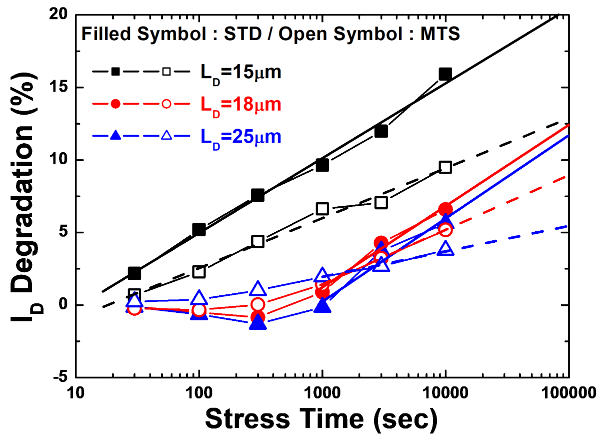
As shown in Fig. 3, shorter drift lengths exacerbate HC degradation in STD devices. For a 15 μm drift length, gm,max degradation was severe, while the MTS device exhibited ~16× higher immunity. Even at longer drift lengths, MTS consistently outperformed the STD design, demonstrating scalability of the reliability benefit.



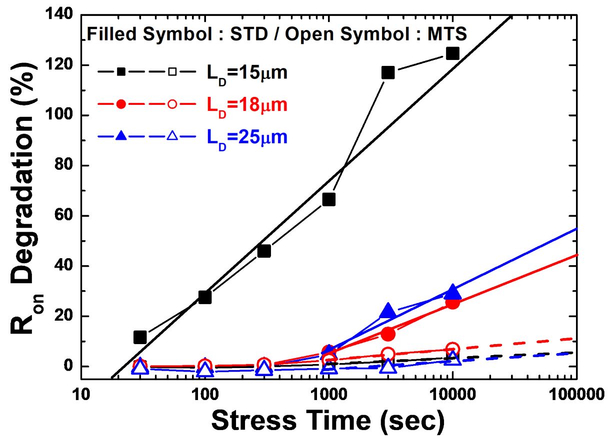
[Fig. 3] Comparison of degradation of maximum transconductance, $g_{m.max}$. of n-LDMOSFETs as a function of stress time. Stress condition is V_{DS}=200V and V_{GS}=5V.

3.3 On-Resistance and Drain Current

Figures 4 and 5 show Ron and drain current degradation under prolonged stress. The STD device exhibited significant deterioration, while the MTS device maintained stable performance. Reduced trap formation and lower peak electric fields in the MTS device directly account for the observed robustness.



[Fig. 4] Comparison of degradation of drain current of n-LDMOSFETs between STD and MTS as a function of stress time. Stress condition is V_{DS}=200V and V_{GS}=5V.



[Fig. 5] Comparison of degradation of R_{on} of n-LDMOSFETs as a function of stress time. Stress condition is V_{DS}=200V and V_{GS}=5V.

3. Conclusion

The multiple trench oxide structure not only improves breakdown voltage but also dramatically enhances hot carrier reliability in SOI LDMOS devices. Compared to standard racetrack source designs, the MTS device demonstrated minimal degradation in gm,max, threshold voltage, drain current, and Ron under prolonged high field stress. These results highlight the dual benefits of the MTS architecture: improved voltage handling capability and superior reliability. The MTS LDMOS thus emerges as a strong candidate for next generation high voltage and high reliability power management ICs.

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